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Design of a High Dynamic-Range RF ASIC for Anti-jamming GNSS Receiver

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ABSTRACT

Global Positioning System (GPS) is used in various fields such as communications systems, transportation systems, e-commerce, power plant systems, and up to various military weapons systems recently. However, GPS receiver is vulnerable to jamming signals as the GPS signals come from the satellites located at approximately 20,000 km above the earth. For this reason, various anti-jamming techniques have been developed for military application systems especially and it is also required for commercial application systems nowadays. In this paper, we proposed a dual-channel Global Navigation Satellite System (GNSS) RF ASIC for digital pre-correlation anti-jam technique. It not only covers all GNSS frequency bands, but is integrated low-gain/attenuation mode in low-noise amplifier (LNA) without influencing in/out matching and 14-bit analog-digital converter (ADC) to have a high dynamic range. With the aid of digital processing, jamming to signal ratio is improved to 77 dB from 42 dB with proposed receiver. RF ASIC for anti-jam is fabricated on a 0.18-μm complementary metal-oxide semiconductor (CMOS) technology and consumes 1.16 W with 2.1 V (low-dropout; LDO) power supply. And the performance is evaluated by a kind of test hardware using the designed RF ASIC.

Keywords: GNSS, anti-jamming, RF ASIC, CMOS, high dynamic-range receiver

1. INTRODUCTION

Global Positioning System (GPS) is a system that has been developed by the U.S. Department of Defense for military purposes. GPS has been actively used in the civilian sector since 2000, and it is currently used in various fields. A GPS receiver is vulnerable to jamming signals because it receives signals transmitted from satellites at about 20,000 km above the Earth and because all the signal characteristics (e.g., frequency, modulation method, and code) are open to the public (Kaplan & Hegarty 2006). The recent GPS jamming from North Korea was a simple type of jamming signal, but it is a strong threat since all the position and time information based on GPS could be disturbed (Hu & Wei 2009). Jamming signals could induce significant disturbance in the civilian fields based on GPS as well as jamming for the military weapon systems. Thus, preparation for this incident is needed. For the removal of jamming signals, various studies have been performed such as an antenna-based anti-jamming technique and a digital signal processing technique (Abimoussa & Landry 2000, Amin & Sun 2005). To apply a technique for the removal of jamming signals, satellite signals that are smaller than thermal noise and jamming signals that are relatively significantly large need to be converted into digital signals without distortion and sent to a jamming removal signal processing part. Therefore, to implement an anti-jamming function, the RF part of a Global Navigation Satellite System (GNSS) receiver needs to have low-noise characteristics as

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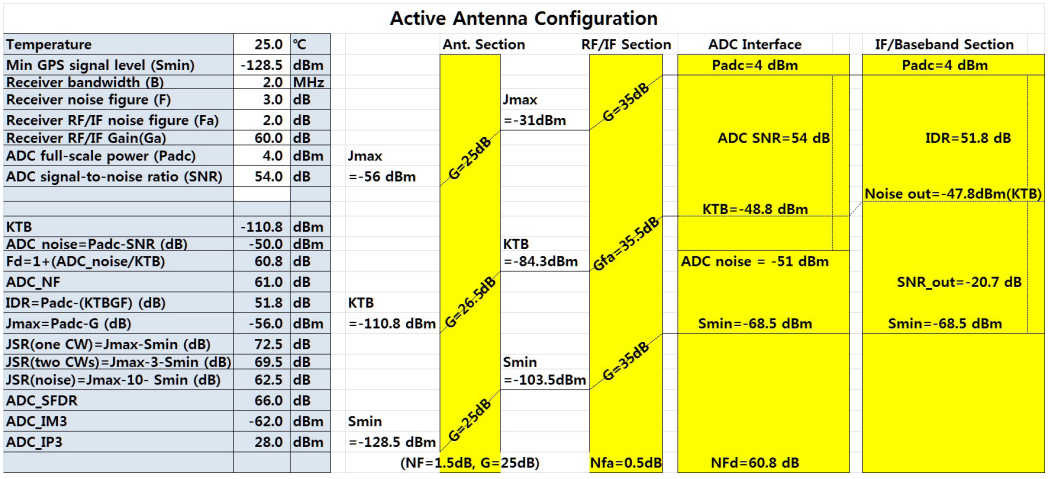

Fig. 1. Design of the dynamic range of RF ASIC.

well as wider dynamic range and linearity compared to an existing general GNSS receiver (Moulin et al. 1998). In this study, high-sensitivity/high-resolution RF ASIC with a wide dynamic range was designed and manufactured so that it could be used for the implementation of a jamming signal removal function, and an anti-jamming device based on digital signal processing that removes narrowband jamming signals in the frequency domain was implemented and the performance was verified.

2. DESIGN OF RF ASIC FOR AN ANTI-JAMMING GNSS RECEIVER

In a general GNSS receiver, the RF front-end appropriately amplifies and filters satellite signals received at a signal strength of about -130 dBm, converts them into digital signals using analog-digital converter (ADC) with effective number of bits (ENOB) of 1.5 ~ 2, and sends them to a digital signal processing part. For satellite signals, the change in the strength of received signals depending on the altitude of satellites is not large (less than 3 dB), and the quantization error can be reduced to less than 1 dB through an appropriate use of AGC. Thus, 2 bit (ENOB) ADC is sufficient for a general GNSS receiver (Parkinson & Spilker 1996). However, an anti-jamming GNSS receiver needs to quantize both satellite signals and jamming signals without distortion and send them to a digital signal processing part even when jamming signals that are more than 50 ~ 70 dB larger than satellite signals are introduced to the receiver along with satellite signals. Therefore, RF ASIC to be implemented should have a wide dynamic range of more than 50 dB and have high-resolution and low-noise characteristics. In general, an anti-jamming receiver uses 12 ~ 14 bit ADC.

2.1 Analysis of the Dynamic Range of RF ASIC

Fig. 1 shows the dynamic range of RF ASIC to be designed in the present study (Moulin et Al. 1998). To implement an anti-jamming function, the full-scale power of ADC (Padc) was set to 4 dBm, and the signal-to-noise ratio (ADC SNR) was set to 54 dB. In the environment shown in Fig. 1, KTB is -110.8 dBm, and the ADC output (noise out) has a value of -47.8 dBm due to the gain and noise characteristics of the antenna and the RF/IF end. In this regard, KTB is the reference thermal noise of IF bandwidth (B) at a room temperature (T=290 K), and K is the Boltzmann constant. Therefore, the dynamic range of the designed RF ASIC was 51.8 dB (IDR = Padc - Noise out), and the jamming-to-signal ratio (JSR) (one CW) was 72.5 dB.

2.2 Design of High-Sensitivity/High-Resolution RF ASIC

Fig. 2 shows the functional block diagram of the high-sensitivity/high-resolution RF ASIC for the implementation of an anti-jamming function. The RF ASIC consists of RF front end, baseband filter that can adjust gain, fractional-N phase-locked-loop (PLL), high-speed 14-bit ADC, and ADC sampling clock generation part. The RF ASIC has two channels; and each channel has a bandwidth of 2~24 MHz for the GPS L1/L2/L5 bands (1575.42/1227.6/1176.45 MHz), a bandwidth of 14/22 MHz for the GLONASS L1/L2 bands (1602.0/1246.0 MHz), and a bandwidth of 32/28 MHz for the GALILEO E1/E5A bands (1575.42/1176.45 MHz). Also, it was designed to have a wide dynamic range by applying high-resolution ADC, RF attenuation block, and variable gain mode low-noise amplifier (LNA). For the output signal of the ADC, Low-Voltage Differential Signaling (LVDS) was applied in order to reduce power consumption and

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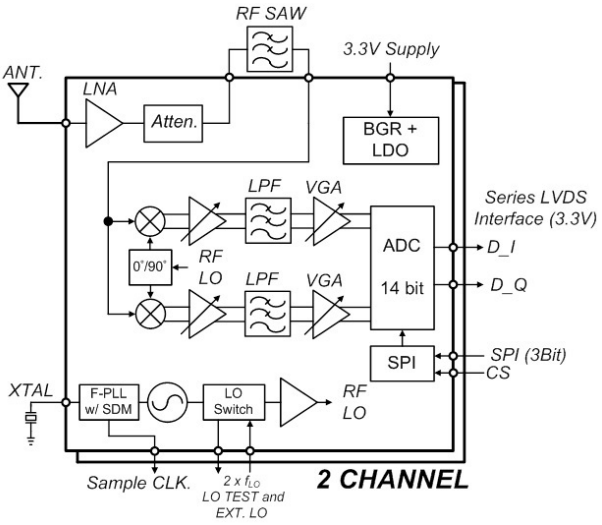

Fig. 2. The proposed 2-channel GNSS receiver architecture.

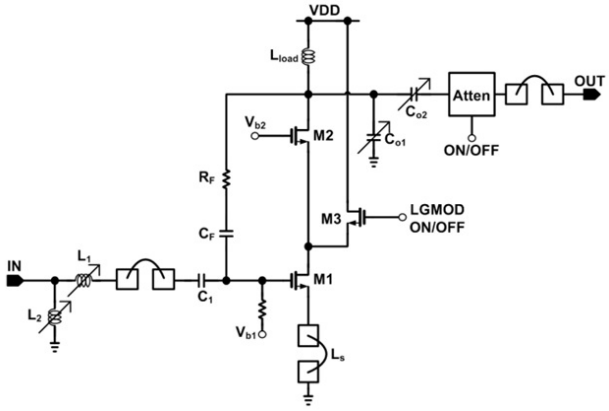

Fig. 3. Circuit diagram of LNA.

to improve noise characteristics. To maintain isolation between each block, low-dropout (LDO) was separately implemented for each channel and block.

2.2.1 RF Front-End and Baseband Filter

In general, a GNSS receiver needs to receive signals that are lower than thermal noise, and thus it should have low-noise characteristics. Also, linearity is also very important for implementing an anti-jamming function. Fig. 3 shows the structure of cascode type LNA, and the feedback components RF and CF play a role in expanding the frequency characteristics. To achieve noise and input matching in LNA at the same time, the conventional inductive source degeneration technique was used. To optimize noise figure, external input matching networks (L1 and L2) need to be properly selected. The input side transistor (M1) provides bias through the internal constant current reference. When a very large jamming signal is introduced, LNA is operated in a low-gain mode by operating M3 in Fig. 3, and saturation of the RF front end is prevented by operating the RF attenuation block. When it is operated in a low-gain mode, a low noise figure can be obtained without affecting the input/output impedance. Also, by integrating the RF attenuation block, a burden for the linearity of the next end mixer can be reduced.

The input impedance of the front-end mixer was set to 50 Ω in order to enable the connection of an external SAW filter. The input of the mixer was implemented based on common-source (CS) and common-gate (CG) stage in order to convert a single-ended signal into a differential signal while having a wide frequency band.

The baseband amplifier (BBA) consists of 7th order Butterworth filter, programmable amplifier, output buffer, and DCOC subloop. The dynamic range of the baseband was implemented to have a value of -12 ~ 52 dB in order to include all the GNSS bands.

2.2.2 Fractional-N Frequency Synthesizer

Each band of the GPS, GLONASS, and GALILEO systems has different frequencies, and thus a frequency synthesizer should include all these bands. For this purpose, a broadband frequency resonant circuit is needed in one VCO and LC-VCO. To make a simple circuit, reduce the area of silicon, and implement a broadband frequency resonator, switched capacitor topology was used. Thus, LC-VCO including 7-bits capacitor banks was designed, and the AFC technique was used (Ko et al. 2005). AFC consists of three blocks: coarse tuning, fine tuning, and dividing blocks. The coarse tuning block corrects VCO frequency using a binary search algorithm. In this regard, an optimal capacitor bank code is searched by comparing the intermediate capacitor bank and the target frequency. To reduce the time for coarse tuning, a binary search algorithm is used. When coarse tuning is completed, the fine tuning block performs tuning based on typical PLL. The proposed VCO has a frequency band of 1.95 ~ 3.45 GHz.

2.2.3 14-Bit ADC

Major performance factors for the implementation of an anti-jamming function include the dynamic range, resolution, and noise characteristics of ADC. In this study, ADC with a 14-bit resolution and a bandwidth of 50MHz was designed and implemented.

The RF front-end has a direct conversion structure, and thus the Nyquist sampling clock of the ADC becomes half of the low-IF structure. The RF ASIC designed in this study

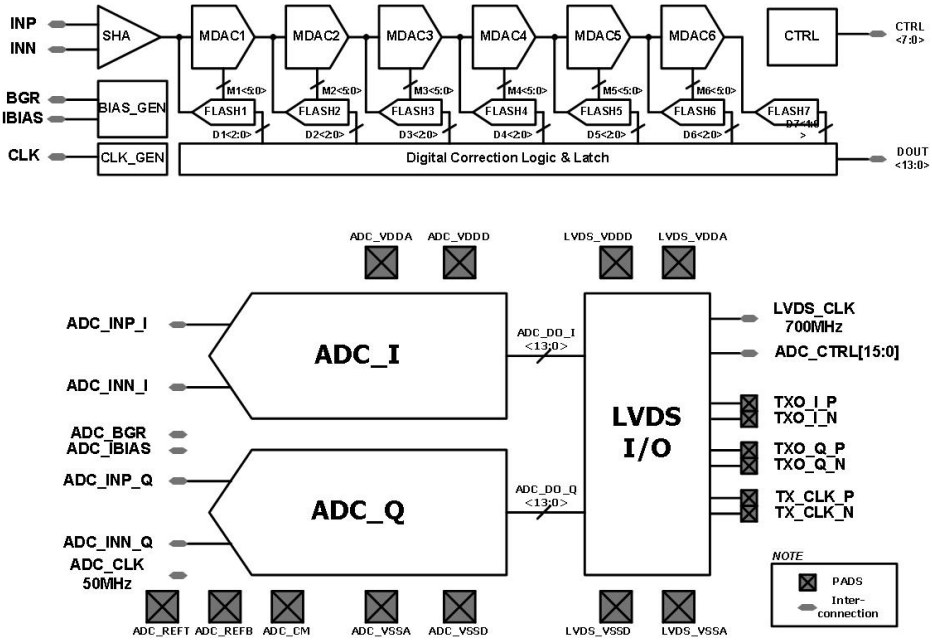

Fig. 4. ADC structure.

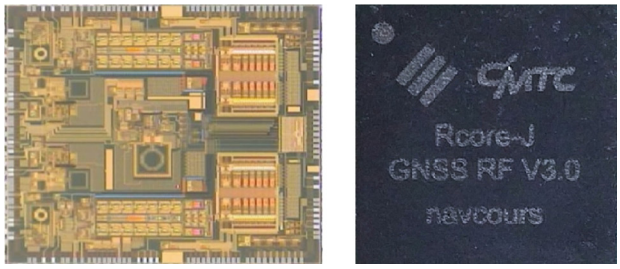

Fig. 5. Fabricated chip and package micro-photograph.

generates 50MHz of clock in ADC PLL, and is sufficient to be used as a sampling clock and to satisfy the GNSS signal band with a maximum of 24 MHz.

ADC consists of sample-and-holder (S/H), pipeline stages, bias block, clock generator, and digital error correction logic block. The input of the ADC was implemented based on a clock bootstrapping switch in order to reduce total harmonic distortion (Fayomi et al. 2004). Fig. 4 shows the ADC structure designed in this study. To implement 14bit resolution and low power consumption, MDAC with a scaling stage structure of 3-3-3-3-3-3-2 was selected. Also, each ADC stage provides digital code for error correction.

3. RF ASIC MEASUREMENT RESULT

The designed RF ASIC was manufactured in a standard 0.18-μm complementary metal-oxide semiconductor

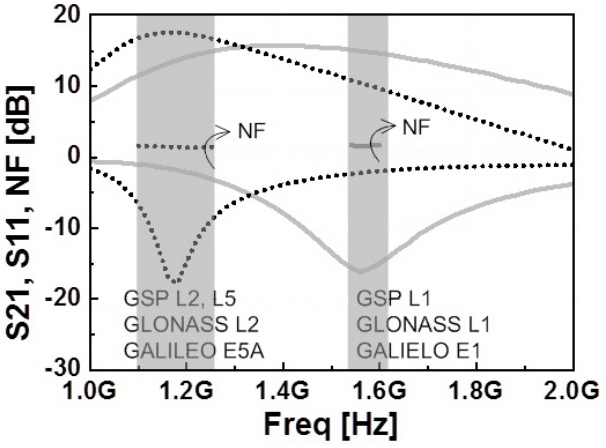

Fig. 6. The measured S-parameter and noise figure of LNA.

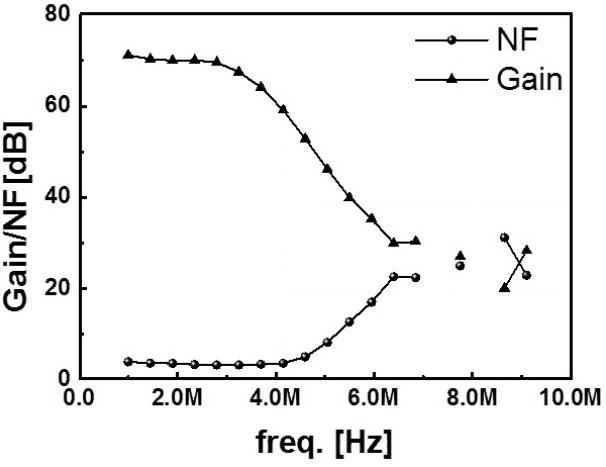

Fig. 7. The measured full-chain gain and NF of RF ASIC.

(CMOS) process. Fig. 5 shows the chip micro-photograph, and it has an area of 5.6 x 5.0 mm including the ESD PAD frame. For the package, a QFN package was used. As shown in Fig. 6, the input reflection coefficient was less than -10 dB for GPS L1 (high band) and GPS L2/L5 (low band) regardless of the high-gain mode or the low-gain mode. The gains were 15.4 dB (high-band) and 17.1 dB (low-band). As shown in Fig. 7, the total gain was 70 dB, but it was 40 dB when there was a jamming signal. The noise figure was 3.2 dB when there was no jamming signal and 4.0 dB when there was a jamming signal.

As shown in Fig. 8, the input P1 dB was -16 dBm and the IIP3 was -7.5 dBm when there was a jamming signal. Also, the dynamic range of the BBA was between -12 dB and 52 dB, and the gain can be adjusted at a 1 dB step. The VCO was between 1.95 GHz and 3.45 GHz, and the tuning range was 55% as shown in Fig. 9. The measured phase noise was -90.9 dBc/Hz for the GPS L1 band at an offset of 100 kHz. The power consumption of the dual-channel RF ASIC was 1.16 W at an input voltage of 2.1 V. Table 1 summarizes the results of the measurement.

4. ANTI-JAMMING FUNCTION IMPLEMENTATION AND PERFORMANCE VERIFICATION

A test bed for the verification of the narrowband anti-jamming function using RF ASIC was implemented as shown in Fig. 10, and the performance was verified. When general RF parts are used, seven to eight chip parts are needed for each channel, and additional matching circuits

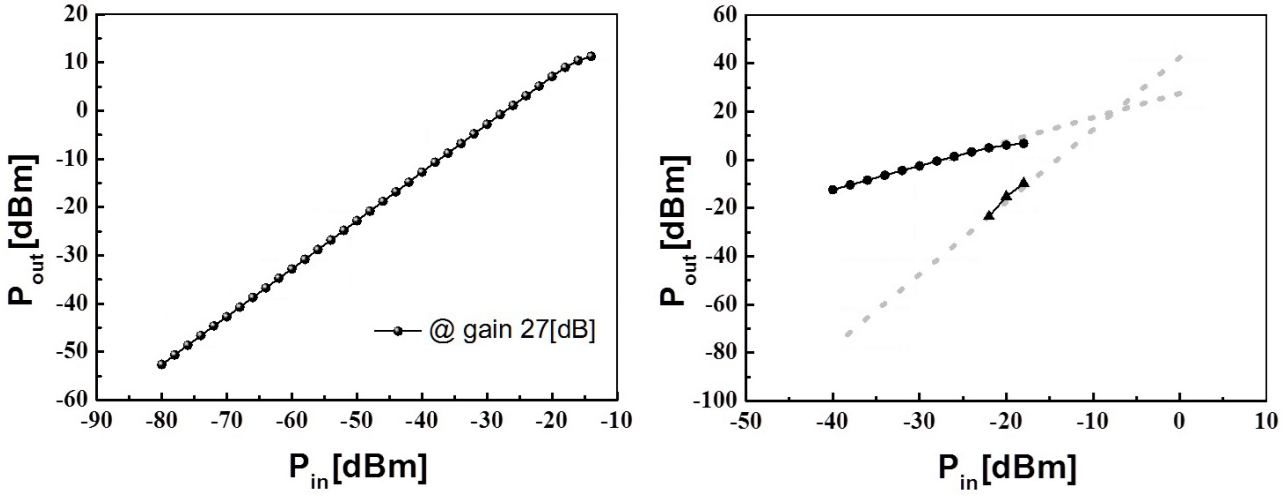

Fig. 8. The measured dynamic range of BBA.

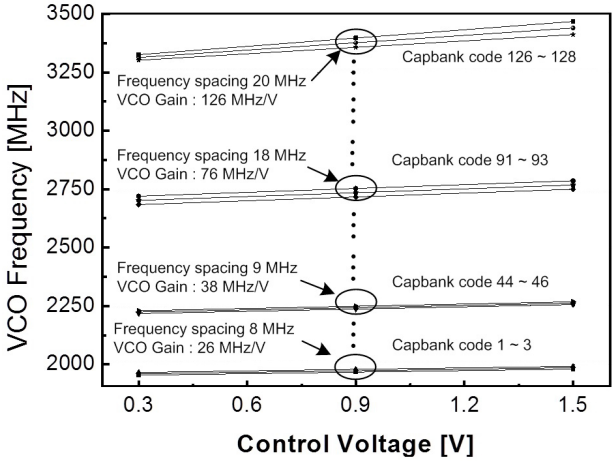

Fig. 9. The measured output frequency range of VCO.

Table 1. Performance summary of RF ASIC.

Block	Parameter	Performance	Unit
	Process	CMOS 0.18	um
	Power	1.16 @2.1V	W
RF front-end	Frequency bands	GPS L1, L2, L5 GLONASS L1, L2 GALILEO E1, E5A	-
	NF @default gain	3.2	dB
	Gain dynamic range	> 81	dB
	Input P1dB @jam. mode	-16	dBm
PLL	Frequency range	1.95 ~ 3.45	GHz
	Resolution	15.3	Hz
	Phase noise	-80/-94/-114 @ 10 k, 100 k, 1 M offset	dBc/Hz
	Fractional spur	-57 @290 kHz	dBc
ADC	Bit resolution	14	Bit
	SNDR/SFDR	54/63	dB/dBc
	Sampling clock	50	MHz

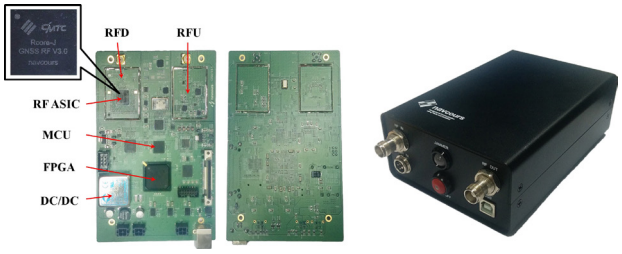

Fig. 10. Test bed for anti-jamming performance evaluation.

and filter parts are needed. The designed RF ASIC was RF/IF two-channel ASIC, and thus only a small number of chip parts were needed and the numbers of filters and passive elements for matching decreased significantly. The area of the RF part of the designed anti-jamming GNSS receiver was about 50% of that of an existing component RF structure.

4.1 Experiment Environment

Fig. 11 shows the experiment environment for the anti-jamming performance verification. The experiment was performed using GPS simulator and signal generator and ProPak-V3 GNSS receiver (NovAtel Inc.). The experiment was conducted using an anechoic chamber. GPS signals and jamming signals generated through the GPS simulator and signal generator were transmitted through each antenna, and the navigation result was measured by receiving the signals using a GPS antenna. Each antenna was installed in the anechoic chamber, and equipment was installed outside so that there would be no jamming signal.

4.2 Experiment Results

When the anti-jamming function was off (w/o anti-jamming) using the test bed, for the GNSS simulator, the input value of the receiving antenna was set to -120 dBm similar to an actual environment. When satellite reception was normally performed, the size of the jamming signal generated through the signal generator was increased, and the size of the jamming signal was measured based on the moment at which the receiver loses satellite navigation (3D navigation). The same experiment was conducted when the anti-jamming function was on (w/ anti-jamming function), and the size of the jamming signal was measured. Then, the difference between the sizes of the jamming signals for the two experiment results would be the anti-jamming performance.

Table 2. The performance of jamming suppressor.

Type of jamming signal	NovAtel receiver (dBm)		Anti-jamming performance (dB)	Remark
	w/o anti-jamming function	w/ anti-jamming function		
CW	-78	-43	35	
AM	-75	-41	34	depth 90%, AM rate 100 Hz
FM	-80	-44	36	dev 2 MHz, FM rate 100 Hz
Sweep CW	-79	-46	33	1574.42 MHz~1576.42 MHz, Point 101, step dwell 2 ms
Pulse	-78	-44	34	Pulse width 450 ms, Pulse Period 500 ms

Table 2 summarizes the results of the same experiment depending on the type of jamming signal (CW, AM, FM, and Sweep CW). These results were obtained by calculating the input value of the receiving antenna considering the antenna cable loss after measuring the size of the jamming signal. In the case of CW, the JSR was 42 dB when only the NovAtel receiver was used, and it was 77 dB when the anti-jamming function was used. Thus, the anti-jamming performance was improved by 35 dB.

5. CONCLUSION

In this study, RF ASIC for the implementation of an anti-

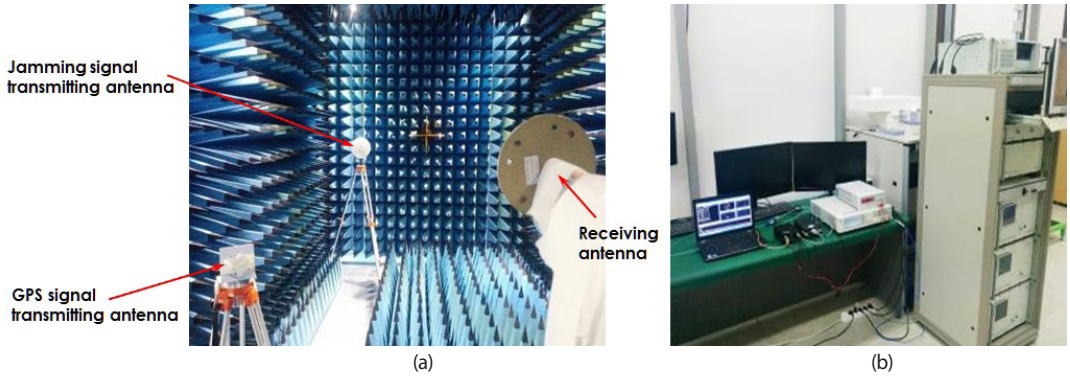

Fig. 11. Anechoic chamber experiment. (a) Internal environment (b) External environment

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Table 3. Performance comparison with other products.

Manufacturers	Tahoe RF	Nu-Trek	RF ASIC of this paper	Unit
Device	TRFS15013	NT/X-Jam/02	RCore-J	
Frequency Band	GPS L1/L2 GLONASS GALILEO	GPS L1/L2/L5 GLONASS L1/L2 GALILEO E1/E5A	GPS L1/L2/L5 GLONASS L1/L2 GALILEO E1/E5A	-
Operating voltage	3.0 ~ 3.6	1.8 & 3.3	2.1	V
Max. gain	75	51	100	dB
Min. gain	35	19	19	dB
Noise Figure @ max. gain	6.0	4.0 (RFE+Mixer only)	3.3	dB
Gain control range	High	19 ~ 51 w/ 1.5 dB step	19 ~ 100 w/ partially 1.0dB step	dB
IIP3	-17		-7.5 @jamming mode	dBm
Input P1 dB	-27(Approx.)	-10	-16.0 @jamming mode	dBm
PLL Jitter	4 psec @ 1 kHz to 30 MHz BW	-	-	-
phase noise	-140 @ VCO, open loop, 10 MHz offset	-	All band around -110 @1 MHz offset	dBc/Hz
Power consumption	1,000 @ 2-channle	1,000 @ 4-channel	1,160 @ 2-Channel	mW
Temp	-40 ~ 85	-30 ~ 125	-40 ~ 85	°C
Feature	- 2 channel GPS receiver - High and Low dynamic range mode - 12bit ADC - No LNA - No LVDS - QFN72 package	- 4 channel GPS RFE - Direct conversion receiver - Up to 40 dB AGC - No ADC - No LVDS - 12 x 12 QFN100 package	- 2 Channel GPS All-band DCR receiver - Fractional-N PLL with 3rd SDM - Wide-band VCO - Variable LPF BW (1~16 MHz) - 14 bit 50 Mb/s ADC - Internal ADC PLL - Serial interface (LVDS) - 10 x 10 QFN68 package	

jamming function was designed and manufactured, and the anti-jamming performance was verified through a test bed. The RF ASIC can be applied to GPS L1/L2/L5, GLONASS L1/L2, and Galileo E1/E5A signal bands, and has two channels in a chip. It has high-speed ADC with a wide dynamic range and high resolution, and the linearity was increased without affecting the input/output impedance by implementing two gain modes of a low-noise amplifier. The general characteristics of the RF ASIC and the JSR performance of the receiver were examined by manufacturing and verifying RF ASIC and by verifying the anti-jamming performance through making a test bed. With the use of the test bed using the RF ASIC, the anti-jamming performance for the narrowband and fractional band of the GPS receiving system could be increased by more than about 35 dB by installing it between the receiving antenna and the receiver in a plug-in form. The RF ASIC developed in this study needs improvements in the dynamic range and noise characteristics in order to improve the JSR performance, but it is thought that the developed RF ASIC would be useful for improving the anti-jamming performance of an existing GNSS receiver by making a smaller anti-jamming device or for the development of a small GNSS receiver with an anti-jamming function. Table 3 compares the performances of existing products and the RF ASIC designed in this study.

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